In the United States Patent and Trademark Office

Date:	August 6, 2006		
In re Application of:	Benayoun, et al.	***Filed:***	12/28/2001
For:	Self-Route Multi-Memory Packet Switch Adapted to have an Expandable Number of Input/Output Ports		
Serial Number:	09/683,432		
Art Unit:	2662	***Examiner:***	Dmitry Levitan

AMENDMENT AFTER FINAL UNDER 37 C.F.R. §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Final Office Action mailed on 6/6/2006, which is due for response by 8/6/2006. Any fees required in entering this response may be charged to Applicant's deposit account, 09-0456.

It is respectfully requested that this Amendment be entered in the above referenced application and reconsideration of the application in view of these comments be made. No new matter has been included. Applicants respectfully request that the following amendments be entered so that the application passes to allowance:

In the Claims

Amend claims 1, 3-5, 7-8, 11- 13, and 15 as follows:

1. (Canceled)

2. (Canceled)

3. (Currently Amended) Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the LANs, the data transmission system comprising:

a packet switch comprising at least a packet switch module interconnecting the plurality of LAN adapters wherein a packet transmitted by any adapter to the packet switch includes a header containing at least the address of the adapter to which the packet is forwarded, the packet switch module includes a plurality of input ports and a plurality of output ports both being respectively connected to the plurality of LAN adapters, each pair of input and output ports defining a cross point within the packet switch module,

wherein the packet switch comprises a memory block for each of the cross points, the memory block including a data memory unit for storing at least a data packet and a first memory controller which determines from the header of the received data packet whether the packet is to be forwarded to the output port associated with the memory block and for storing the data packet into the data memory unit in such a case, and an output control block which includes a scheduler; the scheduler selects a memory block corresponding to the output port and causes the memory block to forward the data packet stored in the data memory unit to the output port when predetermined criteria are met ~~Data transmission system according to claim 1,~~

and wherein the memory block includes a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point, and the first memory controller stores the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to forward it to the output port.

4. (Canceled)

5. (Currently Amended) Data transmission system according to claim 3, further comprising an output data block connected to each output port for storing a data packet received from any memory block and transmitting the data packet to the output port under the control of the scheduler; ~~Data transmission according to claim 4~~,
and wherein the output data block includes a data selection block for validating the data packet after receiving a validating signal from the scheduler, an output memory unit for storing the data packet, and a second memory controller for controlling the operation of storing the data packet into the output memory unit and the operation of reading the output memory unit for transmitting the data packet to the output port.

6. (Canceled)

7. (Canceled)

8. (Currently Amended) Data transmission system according to claim 3, further comprising an input control block connected to each input port for buffering a data packet received from the input port before transmitting the data packet over a distributed data bus connected to all memory blocks corresponding to the input port, wherein the input control block includes an input memory unit for buffering the data packet received from the input port and a third

memory controller which stores the data packet into the input memory unit, and reading the data packet to forward it over the distributed data bus ~~Data transmission system according to claim 7~~,

and wherein the input control block further includes a multiplexer for selecting either the output of the input memory unit or directly the bus connected to the input port when the input control block is not a first switch module of a plurality of switch modules.

9. (Original) Data transmission system according to claim 8, wherein the packet switch includes a plurality of switch modules and wherein each down switch module includes for each output port an input expansion data block for buffering a data packet received from an expansion bus in connected to an up switch module and corresponding to the same output port as the output port of the down switch module.

10. (Original) Data transmission system according to claim 9, wherein the input expansion data block includes an expansion memory unit for buffering the data packet received from the expansion bus in and a fourth memory controller which stores the data packet into the expansion memory unit and reading the expansion memory unit to forward it to the output port of the down switch module.

11. (Canceled)

12. (Currently Amended) Data transmission system according to claim 3, wherein a fourth memory controller sends an overflow signal to a data controller when it has detected that the data memory unit overflows ~~Data transmission system according to claim 11,~~

and further ~~comprising~~ comprises an overflow bus to transport the data packet to the data memory unit of another memory block corresponding to the output port after the data controller has prevented the data packet from being stored into the data memory unit which

overflows and has selected and validated the data memory unit of another memory block which is not overflowing.

13. (Currently Amended) Data transmission system according to claim 12 ~~claim 11~~, further comprising a back-pressure mechanism which sends back-pressure signals to input adapters to request the input adapters to reduce the flow of the data packets transmitted to the packet switch when there is too much overflow detected by one or more of the data controller of the packet switch.

14. (Original) Data transmission system according to claim 13, further comprising an overflow mechanism adapted to receive overflow control signals from the data controller of the packet switch when there is too much overflow and to transmit an overflow signal to the back-pressure mechanism.

15. (Currently Amended) Data transmission system according to claim 3 ~~claim 1~~, wherein the header of the data packet includes two bytes in which the first byte contains an identification field (unicast, multicast) and the second byte contains a module address field when the packet switch comprises several packet switch modules.

Remarks

Claims 1, 3-5, and 7-15 are pending in this action. Claims 1, 4, 7 and 11 stand rejected. By this amendment claims 1, 4, 7, and 11 have been canceled and claims 3, 5, 8-10, and 12-15 have been written in independent form to include the limitations of the rejected base claims and the intervening claims, as suggested by Examiner in the Office Action dated 6/6/2006 on page 5 item 6. Applicants respectfully request reconsideration of all pending claims herein because the dependent claims 3, 5, 8-10, and 12-15 have been rewritten to comply with Examiner's recommendations for allowable claims and because the references cited by Examiner neither teach nor suggest all of the limitations of amended claims 3, 5, 8-10, and 12-15.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that claims 1, 4, 7 and 11 are rejected under 35 U.S.C. § 103(a), as being unpatentable over Holden (US 5,557,607) in view of U.S. Patent No. 6,205,145 issued to Yamazaki and U.S. Patent No. 5,509,008 issued to Genda.

Applicants have canceled claims 1, 4, 7, and 11 and therefore respectfully submit that rejection to claims 1, 4, 7 and 11 under U.S.C. §103(a) has been overcome.

Conclusion

Based on the foregoing, it is respectfully submitted that the claims objected to in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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